Abstract of the Disclosure

A "complete graph" interconnect structure for a hardware emulator for reducing the required programmable interconnect resource in the emulator and using the saved resource to increase the utilization of reconfigurable logic devices, such as field programmable gate arrays (FPGAs), in the emulator and therefore increasing emulator capacity. The device includes a plurality of field programmable gate array devices (FPGAs) having logic and interconnect elements which can be reconfigured for different functions; a "complete graph" interconnect structure having wires connecting all FPGAs together similar to a complete graph and having approximately equal number of wires between any pair of FPGAs; emulation software running on the host computer providing partitioning, routing, the interface to the user and the third party electronic design software, testing and debugging functions; and the support circuit having the downloading, debugging, and testing functions. Any of these signal connecting any pair of FPGAs can be routed with one of the direct connections between the pair of FPGAs on the "complete graph" interconnect structure. Most of the remaining signals can be routed with the one-FPGA route-through paths.